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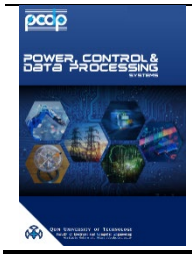

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A Modified Single-Phase Boost AC–AC Converter Using a Switching Cell Topology

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ABSTRACT

This article presents a modified direct single-phase boost AC–AC converter utilizing a switching cell (SC). The main objective is to eliminate voltage stress and minimize the size of magnetic components. The suggested non-isolated converter has a very straightforward design, which employs two inductors. The suggested design eliminates the need for DC link and provides boost capability with simple control. Furthermore, the proposed topology reduces current levels and mitigates body-diode recovery issues, which in turn decreases switching and conduction losses and effectively minimizes the losses associated with MOSFET body-diode recovery. Therefore, this converter represents a practical option for many applications, such as renewable energy systems, energy storage systems, and microgrids. To improve this system's reliability and efficiency, exact and steady power regulation is essential in these domains. The operational principles of the recommended converter in various modes are analyzed comprehensively, and based on the results of the simulation in MATLAB/Simulink. Finally, the suggested converters' performance accuracy is confirmed by simulation analysis at 20V input, D = 0.7, 50kHz switching frequency, 122V output, and 150W output power.

Keywords: Step-up AC-AC converters; Switching cell; Non-isolated converters; Continuous input current.

1 Introduction

Because of rapid growth and changes in energy demand, along with the ongoing addition of large renewable energy sources to the grid, many power quality problems. These include utility voltage drops and rises, flickering voltage, and imbalances in the three-phase system [1]. Voltage sags and swells represent major problems, especially for end users managing sensitive loads linked to the grid. This is especially true when viewing the problem from the perspective of the utility [2]. The failure of electrical equipment, the damage of sensitive devices, the loss of computer data, and an increase in line losses are caused by voltage sags and swells.

Moreover, keeping stability and dependability has become more challenging as contemporary power systems progress toward smart grid operation and larger penetration of renewable energy sources. For instance, in renewable-integrated systems, islanding detection depends significantly on detecting generator coherence groups [3]. Similarly, there has been a lot of focus on improving the efficiency of integrated energy hubs [4] and controlling the energy use of smart homes utilizing smart algorithms [5]. These results illustrate the increasing significance of adaptive and high-performance power conversion systems that can manage changes and inflexible grid factors.

In this context, AC–AC converters have emerged as viable solutions for keeping voltage stability, modifying for power interruptions, and assuring reliable operation under dynamic grid settings. The various topologies of these converters can be classified into three main categories: AC-DC-AC converters, matrix converters, and direct pulse-width modulation (PWM) AC-AC converters. AC-DC-AC converters can produce both raised and decreased outputs, rendering them appropriate for diverse applications, including motor drives and renewable energy systems. Nonetheless, its dual-stage conversion method (AC-DC followed by DC-AC) results in increased power losses, decreased efficiency, and higher system complexity [6]. A sizable and short-lived electrolytic capacitor in the DC link exacerbates overall dimensions, expenses, and maintenance demands. Furthermore, the requirement for an input power factor corrector complicates the control technique. These converters are generally restricted to voltage step-down capabilities, rendering them inadequate for specific applications. Matrix converters (MCs) are a type of AC-AC converters that may directly modify output frequency without requiring major DC-link capacitors, hence providing compactness and improved reliability [7]. However, MCs that change frequency in steps have trouble producing smooth sinusoidal output voltages, which may limit their use in sensitive situations. Despite this, they are widely used in systems that need adjustable voltage and frequency, such as motor drives [8], medium-frequency transformer isolation for traction, and dynamic voltage restorers (DVR), taking advantage of their small size and fast switching abilities [9]. The direct PWM AC-AC converter is a one-step power conversion method that doesn't need a direct current link, which has greatly improved its efficiency. This converter, motivated by the need for voltage amplitude regulation, is of interest and should be continually investigated [10, 11]. To be more specific, it is more appealing for applications of this kind, which only require the grid voltage amplitude to be maintained without simultaneously changing the phase shift and frequency. Among several types of AC-AC converters, direct PWM AC-AC converters are considered a more appropriate choice for voltage range adjustment due to their single-stage conversion, compact size, and ease of control. Direct PWM AC-AC converters include several topologies, such as Z-Source converters [12], buck converters [13], boost converters [14], buck-boost converters [15], and multilevel converters [16]. Each configuration presents distinct advantages based on the specific application needs. Z-Source converters are known for their ability to increase and reverse voltage in one step, making them more reliable and better at resisting electromagnetic interference [17]. Buck and boost converters are commonly utilized for their structural simplicity and efficiency in voltage reduction or elevation, respectively. Buck-boost converters include the functions of both buck and boost processes, rendering them appropriate for applications with extensive input/output voltage fluctuations. Multilevel converters improve the quality of the output waveform, lower the voltage stress on devices, and decrease total harmonic distortion (THD), making them ideal for high-power uses. The different designs of these converters make direct PWM AC-AC converters more flexible, helping them meet the needs of today's power systems that have various voltage levels and efficiency requirements. Direct AC-AC converters are preferred for their single-stage design, diminished component quantity, and elevated conversion efficiency. These attributes enable a streamlined system architecture, reduced production expenses, and improved reliability [18]. The buck-boost AC-AC architecture is the most developed among direct converters, including both step-up and step-down voltage conversion capabilities; hence, it is expanding its range of applications. Conversely, direct buck and boost AC-AC converters have garnered relatively less focus and demonstrate more constrained capabilities. This work focuses on direct step-up AC-AC converters. Moreover, in the following, recent breakthroughs and design enhancements in this category are investigated to underscore its comparative benefits and possible application domains [2].

In 2005, Peng et al [7, 19] originally presented the direct AC-AC converter topology by substituting the unidirectional switches and diodes in the conventional Z-source converter with bidirectional switches. This alteration produced a gain of $(1\text{-}D)/(1\text{-}2D)$ and facilitated buck-boost operation. This converter employs merely two power switches; nevertheless, the significant voltage stress on these switches requires the use of snubber circuits. Additionally, the input current waveform in this converter is not smooth, so an input filter is needed to reduce unwanted current harmonics. To resolve this issue, Nguyen et al [7, 20] proposed the quasi-Z-source (qZS)

architecture, which integrates an input-side inductor to maintain continuous input current. The trans-ZS setup uses a connected inductor instead of a regular inductor like in the usual qZS, which improves the voltage conversion ratio. However, the scope of the duty cycle is constrained, as indicated in [7, 21]. A Γ-source AC–AC converter that employs merely two power switches and four passive components has presented in [22]. This converter, unlike many earlier designs that use impedance sources, provides a steady input current and operates in both boost and buck modes. Moreover, it attains a maximum efficiency up to 90%.

Recent years have seen the introduction of a new AC–AC converter topology that employs four power switches [23]. This converter utilizes a novel method by integrating four series-connected diodes, each aligned in series with a MOSFET. This design effectively eliminates energy losses and reduces the issues caused by the MOSFET body diodes, which are common problems in older converters that often result in lower efficiency and more complicated snubber circuits. As a result, this design attains an exceptional efficiency up to 95%, rendering it very appropriate for high-efficiency applications. The proposed converter provides substantial operational flexibility; it is capable of operating in buck, boost, and buck-boost modes. This adaptability allows for its use in diverse AC power systems necessitating different voltage conversion profiles. Moreover, Sharifi et al.[24] enhanced a switching network by creating an AC–AC converter integrated with a Z-source impedance network, intended for operation across an extensive voltage range. A main advantage of this design is that it provides a specific path for freewheeling current, which means there is no need for extra snubber circuits usually found in Z-source AC–AC converters. The elimination of snubber circuits decreases both the overall dimensions and expenses of the converter while substantially decreasing power losses. This topology offers a compelling blend of high efficiency, improved operational flexibility, and streamlined design, rendering it an optimal choice for contemporary power electronics applications.

This paper introduces an innovative direct step-up AC-AC converter utilizing a switching-cell topology. The design markedly minimizes magnetic component size and weight and enhances overall efficiency. The converter exhibits continuous input and output current waveforms, which can reduce harmonic distortion and enhance power quality. The output voltage preserves the input voltage's phase and frequency, while its amplitude can be adeptly regulated by duty cycle modulation. This attribute renders the converter especially appropriate for applications involving inductive power transmission from low-voltage AC sources. These features make the proposed converter a good choice for advanced AC power conditioning systems that need to efficiently increase voltage in a compact design.

The paper remaining sections are organized as follows: configuration of the suggested converter is explained in section 2. In section 3, operating states of the converter are described. Design procedure of components and performance analysis of the proposed converter are presented in section 4. Section 5 gives simulation results that demonstrate the effectiveness of the suggested topology. Finally, section 6 derives the conclusions.

2 Proposed Converter Topology

Figure 1 illustrates the configuration of the proposed single-phase boost AC–AC converter. This converter is designed to step up voltage, enhancing power quality while minimizing component count. The circuit consists of multiple energy storage components, namely four inductors (L_1, L_2, L_3, and L_4), which are optimally positioned to regulate magnetic energy transmission and mitigate current ripple. Furthermore, three capacitors (C_{in}, C_1, and C_O) are employed for voltage enhancement, energy storage, and output voltage purification, respectively. The power conversion is enabled by five semiconductor switches. Switch S operates as a bidirectional switch controlled by high-frequency PWM, allowing current to flow in both directions and enabling smooth AC–AC conversion. The switches are essential for determining the converter's operational states and managing the duty cycle to regulate voltage gain.

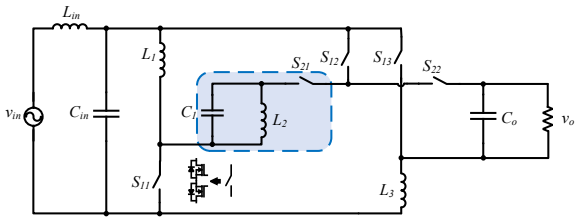


Figure 1: Schematic of the proposed boost AC-AC converter.

3 Descriptions of Operating Modes

Figure 2 depicts the switching waveforms and modulation approach used for the bidirectional power switches. These waveforms are shown during both the positive and negative half-cycles of the input voltage source.

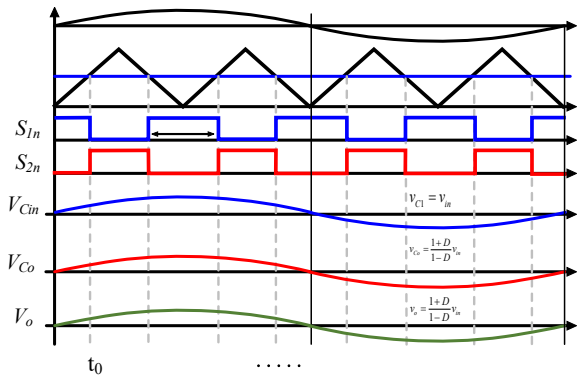


Figure 2: PWM switching diagram of the proposed AC-AC boost converter configuration, provided with the waveforms of output and capacitor voltages.

The voltage that is produced as a result stays in phase with the voltage that is input, which guarantees that the operation is synchronized during the whole AC cycle.

The proposed converter applies a switching way that employs PWM to ensure efficient power conversion and accurate regulation of output voltage amplitude and frequency. The suggested converter generates high-frequency PWM signals by comparing a reference waveform with a high-frequency triangular carrier wave.

This comparison outcome dictates the switching moments of the semiconductor devices. When the S_{1n} switches are engaged, the converter operates in mode I, while activating the S_{2n} switches leads to operating in mode II, which is shown in Fig. 3 and discussed in the following.

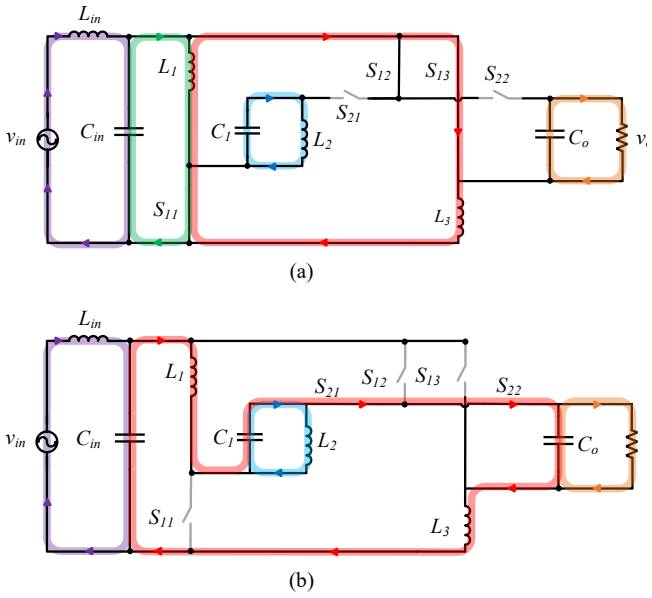


Figure 3: Equivalent circuits of the proposed topology in operating modes; (a) mode I (DTs), (b) mode II (1-D)Ts.

Mode I ($0<t<DTs$): During this mode, switches S_{11}, S_{12}, and S_{13} are on, while switches S_{21} and S_{22} stay deactivated. Consequently, the input inductor L transitions into the energy storage phase, resulting in an increase in its current due to the applied input voltage. By applying KVL for the equivalent circuit (as shown in Fig. 3(a)) in this mode, the following equations are obtained:

$$\begin{aligned} v_{Lin} &= L_{in}\frac{di_{Lin}}{dt} = v_{in} - v_{Cin} \\ v_{L1} &= L_1\frac{di_{L1}}{dt} = v_{cin} \\ v_{L1} &= L_1\frac{di_{L1}}{dt} = v_{L3} \\ v_{L2} &= L_2\frac{di_{L2}}{dt} = v_{C1} \\ v_{Co} &= v_o \end{aligned} \qquad \text{Eq 1}$$

The current increase in the inductors in mode I is as follows:

$$\begin{aligned} \Delta i_{Lin} &= \frac{v_{in} - v_{Cin}}{L_{in}} DT_s \\ \Delta i_{L1} &= \frac{v_{cin}}{L_1} DT_s \\ \Delta i_{L1} &= \frac{v_{L3}}{L_1} DT_s \\ \Delta i_{L2} &= \frac{v_{C1}}{L_2} DT_s \end{aligned} \qquad \text{Eq 2}$$

Mode II ($DT_s<t<T_s$): In this operation mode, switch S_1 is off, and S_2 is on. Unlike the previous mode, the inductors L_{in} and L_1 are in the discharging state, while the capacitors C_1 and C_O are being charged. In mode II, by applying KVL for the equivalent circuit (as depicted in Fig. 3(b)), the following equations are obtained:

$$\begin{aligned} v_{Lin} &= L_{in}\frac{di_{Lin}}{dt} = v_{in} - v_{Cin} \\ v_{L1} &= L_1\frac{di_{L1}}{dt} = v_{Cin} + v_{C1} - v_o - v_{L3} \\ v_{L2} &= L_2\frac{di_{L2}}{dt} = v_{C1} \\ v_{Co} &= v_o \end{aligned} \qquad \text{Eq 3}$$

In mode II, the current increase in the inductors is as follows:

$$\begin{aligned} \Delta i_{Lin} &= \frac{v_{in} - v_{Cin}}{L_{in}}(1-D)T_s \\ \Delta i_{L1} &= \frac{v_{Cin} + v_{C1} - v_o - v_{L3}}{L_1}(1-D)T_s \\ \Delta i_{Lin} &= \frac{v_{C1}}{L_2}(1-D)T_s \end{aligned} \qquad \text{Eq 4}$$

The volt-second balance law is applied for determination of the voltage gain M_{boost} as follows:

$$M_{Boost} = \frac{v_o}{v_{in}} = \frac{1+D}{1-D} \qquad \text{Eq 5}$$

The calculated voltage gain expressions offer information about the performance of the proposed converter under varying operating conditions. As derived, the gain is dependent on the duty cycle of the converter. Figure 4 shows the converter voltage gain versus duty cycle.

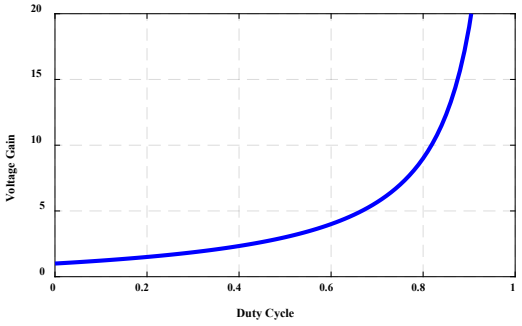


Figure 4: Converter voltage gain versus duty cycle.

4 Components Design

For inductors L_1 - L_4, two energy storage capacitors C_{in} and C_1, and the output filter capacitor C_O, the minimum requisite inductance or capacitance values are calculated based on the maximum inductance-current ripple or capacitance voltage ripple values, respectively. Based on the aforementioned points, the peak values of the voltage and the inductors current are obtained as follows:

$$i_{(Lin)Peak} = \frac{1+D}{1-D} i_o$$
$$i_{(L1,L3)Peak} = \frac{1}{1-D} i_o \quad \text{Eq 6}$$
$$i_{(L2)Peak} = i_o$$

$$v_{Lin} = \frac{(1-2D)}{1+D} v_o$$
$$v_{L1,L3} = \frac{D}{1+D} v_o \quad \text{Eq 7}$$
$$v_{L2} = v_{C1}$$

The inductance values L_{in}, L_1, L_2 and L_3 needed for sustaining the maximum current ripple at $\Delta i_L = x.i_L$, with x varying from 20% to 40%, can be ascertained as follows:

$$L_{in} \geq \frac{(1-2D)}{(1+D)\Delta i_{Lin} f_s} v_o$$
$$L_1, L_3 \geq \frac{D^2}{(1+D)\Delta i_{Lin} f_s} v_o \quad \text{Eq 8}$$
$$L_2 \geq \frac{D}{\Delta i_{L2} f_s} v_{L3}$$

To determine the capacitance value, it is necessary to calculate the current flowing through the capacitor, which is similar to the output current in the chosen operating modes. Furthermore, the voltage across the capacitors can be determined using the following equation:

$$v_{Cin} = \frac{1-D}{1+D} v_o$$
$$v_{C1} = v_{L3} \quad \text{Eq 9}$$
$$v_{Co} = v_o$$

The capacitors C_{in}, C_1, and Co values are selected to minimize the maximum voltage ripple to $\Delta v_C = y.v_C$, where v_C indicates the maximum voltage stress on the capacitor, and y varies between 5% and 10%. So that the Δv_C stays within the set limits, the requisite minimum values for capacitors C_{in}, C_1, and C_O can be determined as follows:

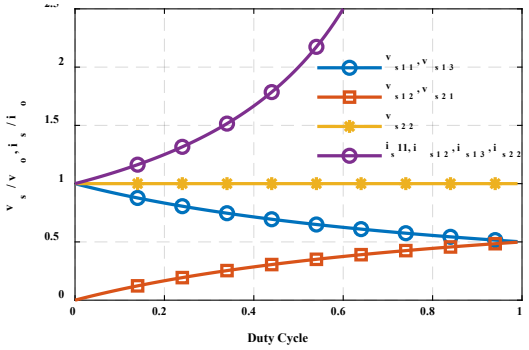
$$C_{in} \geq \frac{D}{\Delta v_{Cin} f_s} i_o$$
$$C_1 \geq \frac{D}{\Delta v_{C1} f_s} i_o \quad \text{Eq 10}$$
$$C_o \geq \frac{D}{\Delta v_{Co} f_s} i_o$$

The voltage and current stress are the two most important factors that are considered while selecting power semiconductor switches. The following is a description of the voltage and current stress that occurs by all of the active components in the proposed converter. The rate of voltage and current stress in each semiconductor switch is shown in (11) and (12).

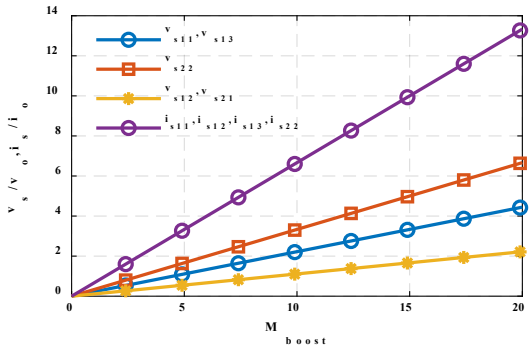
$$v_{S11} = v_{S13} = \frac{1}{1+D} v_o$$
$$v_{S12} = v_{S21} = \frac{D}{1+D} v_o \quad \text{Eq 11}$$
$$v_{S22} = v_o$$

$$i_{S11} = i_{S13} = i_{S12} = i_{S21} = i_{S22} = \frac{1}{1-D} i_o \quad \text{Eq 12}$$

Figure 5 compares the voltage and current stresses relative to the output voltage and current across switches S_{11} to S_{22} for varying duty cycles and voltage gains. Figure 5(a) demonstrates that the voltages of switches S_{13} and S_{12} constantly decrease with a higher duty cycle, but the voltage of switch S_{22} is constant throughout all duty cycles. Moreover, the switches S_{12} and S_{21} currents and the voltages continue to rise with an increase in the duty cycle. Figure 5(b) illustrates that when the voltage gain increases, the curves have increasing slopes and indicate a rising trend. Moreover, Table 1 provides an overview of the analyzed elements.



(a)



(b)

Figure 5: Comparison of voltage and current stress; (a) switches voltage and current stress versus D, (b) switches voltage and current stress versus Mboost.

Table 1: Voltage and current stresses of converter components.

Parameter		*Proposed Topology*
M_{boost}		$\frac{1+D}{1-D}$
Device voltage & current stresses	v_S	$v_{S11}=v_{S13}=\frac{1}{1+D}v_o$ $v_{S12}=v_{S21}=\frac{D}{1+D}v_o$ $v_{S22}=v_o$
	i_S	$i_{S11}=i_{S13}=i_{S12}=i_{S21}=i_{S22}=\frac{1}{1-D}i_o$
Input/output inductor current stresses	i_L	$i_{(Lin)Peak}=\frac{1+D}{1-D}i_{o,Peak}$ $i_{(L1,L3)Peak}=\frac{1}{1-D}i_{o,Peak}$ $i_{(L2)Peak}=i_{o,Peak}$
Capacitor voltage stress	v_C	$v_{Cin}=\frac{1-D}{1+D}v_o$ $v_{C1}=v_{L3}$ $v_{Co}=v_o$

$$I_{(S11,S12,S13,S21,S22)\_rms}=\frac{\sqrt{D}}{(1-D)}I_{o\_rms}$$
$$I_{Lin\_rms}=I_{in\_rms}$$
$$I_{L1\_rms}=I_{o\_rms}\sqrt{\frac{D}{(1-D)^2}+(1-D)}$$
$$I_{L2\_rms}=I_{o\_rms}$$
$$I_{L3\_rms}=I_{o\_rms}\sqrt{D(\frac{1}{1-D})^2+(1-D)}$$
$$I_{Cin\_rms}=I_{o\_rms}\sqrt{D(1+\frac{1}{1-D})}$$
$$I_{C1\_rms}=I_{Co\_rms}=I_{o\_rms}\sqrt{\frac{1}{(1-D)}(\frac{D}{(1-D)}+D^2)}$$
Eq 13

5 Power Loss Analysis

To reduce the complexity of power loss analysis, some assumptions are considered. First of all, active and passive components exhibit entirely symmetric characteristics. Secondly, the approach ignores inductance-current ripple and capacitance-voltage ripple. The formulas for RMS current values in switches, inductors, and capacitors are as follows as shown in Eq. (13).

5.1 Conduction Losses

Conduction losses include the winding losses associated with the inductors L_{in}, L_1, L_2, and L_3. These losses occur as a result of the conduction of current through the inductor windings, which generates resistive heating due to the equivalent series resistance (ESR) of the coils. Consequently, the total power loss, $P_{W,\text{Cond.}}$, can be expressed as follows:

$$P_{W,Cond}=(I_{L,rms})^2 r_w \qquad \text{Eq 14}$$

where $I_{L,rms}$, indicates RMS current of the inductor and r_w denotes its winding resistance. RMS currents are given in (13).

5.2 Capacitor Losses

The capacitor loss $P_{C,\ ESR}$ is caused by the equivalent series resistance of capacitors C_{in}, C_1, and C_O, which can be calculated as follows:

$$P_{C,ESR}=(I_{C,rms})^2 r_{C,ESR} \qquad \text{Eq 15}$$

where $I_{C,rms}$ indicates the RMS current of the capacitor and $r_{C,rms}$ represents the appropriate series resistance. The RMS current of the capacitors is calculated by (13).

5.3 Switches Losses

Power MOSFETs show resistive conduction loss, denoted as $P_{S,Cond}$, which is calculated as given in the following:

$$P_{S,Cond}=(I_{S,rms})^2 r_{S,ON} \qquad \text{Eq 16}$$

where $I_{S,rms}$ indicates the MOSFET's RMS current and $r_{S,ON}$ denotes on-resistance of the MOSFET. The major power loss of MOSFETs is switching loss (P_{Sw}) caused by the discharge of their junction capacitor, which is determined as follows:

$$P_{SW}=f_s.E_{oss}.V_s \qquad \text{Eq 17}$$

E_{oss} represents the quantity of energy lost during capacitive turn-on, as specified in the device datasheet. V_s denotes the blocking voltage of the MOSFET.

Finally, P_{Loss} includes conduction loss, switching losses, and capacitor losses that is formulated as given in the following:

$$P_{Loss}=P_{W,cond}+P_{C,ESR}+P_{S,cond}+P_{Sw} \qquad \text{Eq 18}$$

The efficiency of the converter is determined as follows:

$$\eta=\frac{P_o}{P_o+P_{Loss}}\times 100 \qquad \text{Eq 19}$$

6 Comparison Study

Table 2 shows the results of a comparison between the suggested converter and five recently published types of boost AC-AC converters.

Although, the suggested converter has lesser gain than the improved switched inductor (ISL) based converter presented in [25], but it provides higher voltage gain than other converters, as given in figure 6.

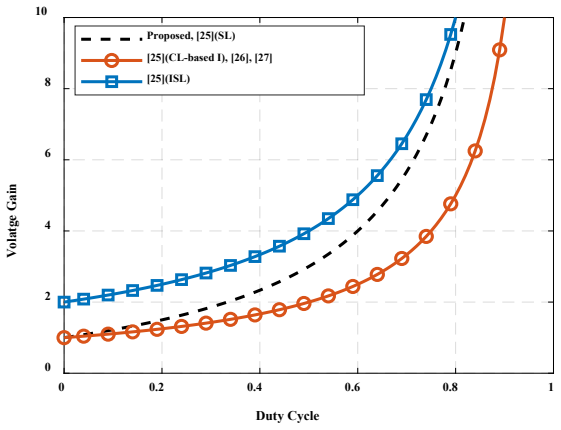


Figure 6: Voltage gain of the compared converters.

Table 2: Comparison of the proposed converter with similar boost AC-AC converters.

	Proposed	[27]	[26]	[25] (SL)	[25] (ISL)	[25] (CL-based I)
Voltage Gain	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1+D}{1-D}$	$\frac{2}{1-D}$	$\frac{1}{1-D}$
Number of MOSFETs	5	4	6	4	4	4
Number of Diodes	0	6	8	9	8	7
Number of Capacitors	3	2	2	1	2	2
Number of Inductors	4	0	1	2	2	1
Total switches voltage stress/ $\sqrt{2}V_{in,RMS}$	$\frac{3+3D}{1-D}$	$\frac{4}{1-D}$	$\frac{6-2D}{1-D}$	$\frac{4+4D}{1-D}$	$\frac{4+4D}{1-D}$	$\frac{4}{1-D}$
Total switches current stress/ $\sqrt{2}I_{o,RMS}$	$\frac{5}{1-D}$	NA	$\frac{3}{1-D}$	$\frac{8}{1-D}$	$\frac{4+4D}{D(1-D)}$	$\frac{4}{1-D}$
Continuous input current	Yes	Yes	Yes	Yes	Yes	Yes

Figure 7a shows that the voltage stress of the suggested converter is lower than that of the introduced converters (SL and ISL) in [25] and [26]. Furthermore, when the duty cycle is below 0.33, the voltage stress of the suggested converter is lower than that provided in [27] and coupled inductor based (CL-based I) converter of [25]. As shown in Figure 7b, except for the CL-based I and [26] converter, the current stress of the total semiconductors in the suggested topology is lower than the other proposed topologies in [25].

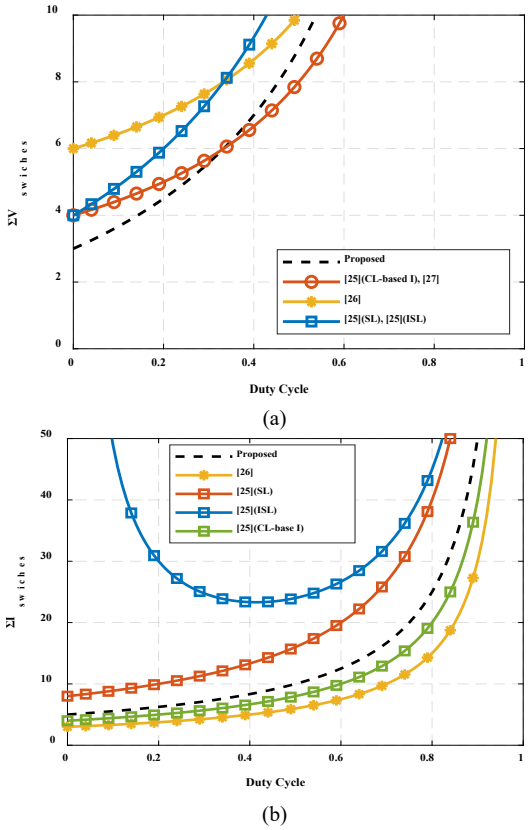


Figure 7: Comparison of total stress of semiconductors; (a) voltage (b) current

Furthermore, in comparison with existing comparable converter topologies, the suggested converter exhibits reduced overall semiconductor stress that improve it for practical applications. Therefore, the proposed converter is a suitable topology, offering adequate voltage gain, modest component count, and low device voltage stress.

7 Simulation Results and Discussion

In this section, the proposed AC–AC converter is simulated using MATLAB/Simulink to verify its performance and theoretical analysis. The component values employed in the simulation model, are summarized in Table 3. If the input voltage peak, V_{in}, is set to 20V then the output voltage peak V_O is capable of reaching to approximately 112V at a frequency of 50 Hz when the duty cycle is adjusted to 70%.

Table 3: Simulated Converter Specifications

Parameters	Values
V_{in}	20V/50Hz
Duty cycle (D)	70%
Switching frequency	50kHz
Inductor L_{in}	1.5mH
Inductors L_1, L_3	100μH
Inductor L_2	50μH
Capacitor C_{in}	47μF
Capacitor C_1	1μF
Capacitor C_o	100μF
Output power	150W
Output voltage	112V
R_{load}	40Ω

Figure 8 illustrates the switching signals corresponding to the semiconductor devices of the converter, including S_{1N} and S_{2N}, where the subscript "N" denotes the number of the switch in each operating mode. These waveforms provide a clear

representation of the switching strategy and validate the accurate operation of the proposed topology.

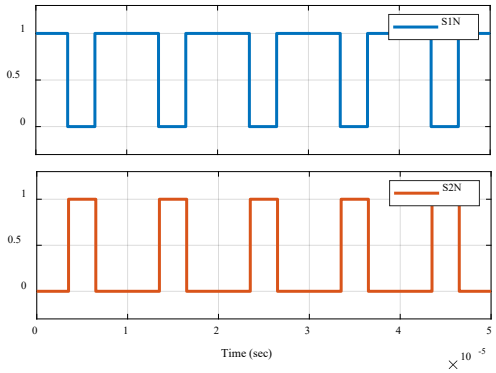
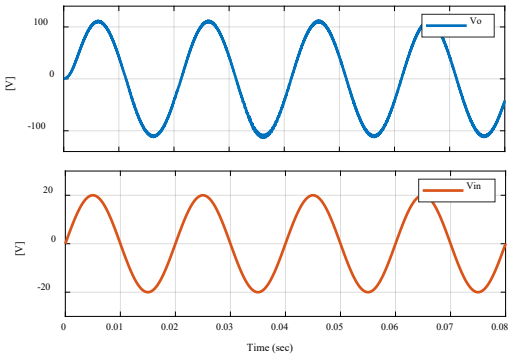
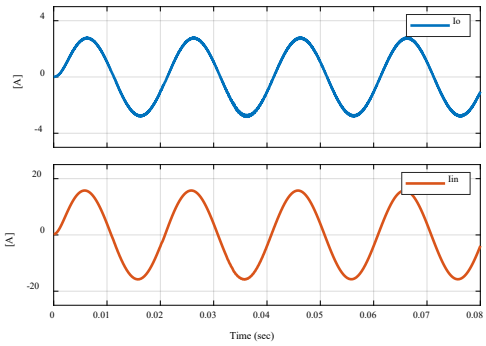


Figure 8: Switching states of the semiconductors

As a result, the two generated signals exhibit no delay, and so the proposed AC–AC converter operates without the need for dead-time, fully consistent with its theoretical analysis. Figure 9(a) shows the waveforms of the input voltage, V_{in}, and output voltage, V_O, while figure 9(b) shows the waveforms of the input current, I_{in}, and output current, I_O. It is clear that the input current is nearly ripple free.
align with waveforms at the circuit level.



(a)



(b)

Figure 9: Input/output waveforms of the proposed converter (a) Input and output voltage waveforms (b) Input and output current waveforms

Additionally, figure 10 and figure 11 show the voltage waveform of capacitors C_1 and C_O, and the switch voltage signals, respectively. The switch voltage waveforms indicate that the switches do not undergo high voltage stress that confirms the low-stress and reliable operation of the proposed AC–AC converter, contributing to reduced switching losses and enhanced component longevity.

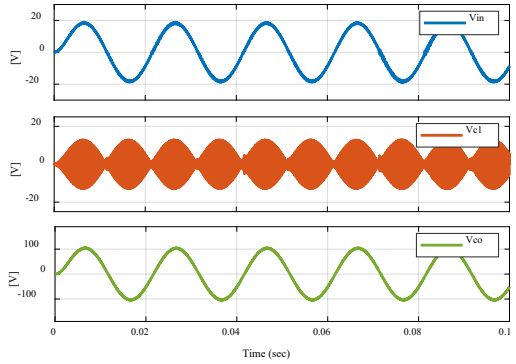


Figure 10: Capacitors C_1 and C_o voltage waveforms

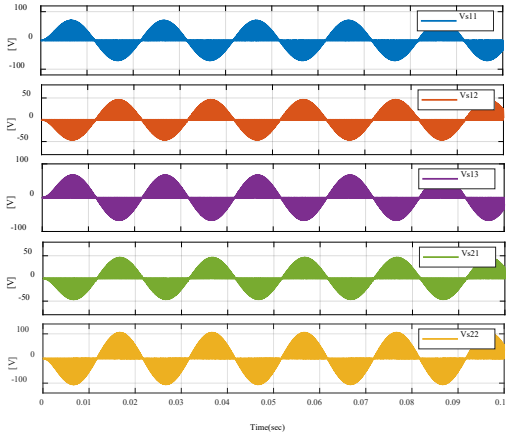


Figure 11: Voltage waveforms of the converter switches

Figure 12 displays the current waveforms of the inductors L_1 and L_2. Figure 13 illustrates the current waveforms of the switches. The waveforms indicate no excessive voltage or current surges, in agreement with the previous theoretical analysis. In addition to validate the suggested topology, the simulation results support the analytical model. The suggested converter retains its anticipated step-up capability and voltage regulation, and the obtained steady-state relations for voltage gain, inductor currents, and semiconductor stresses strongly

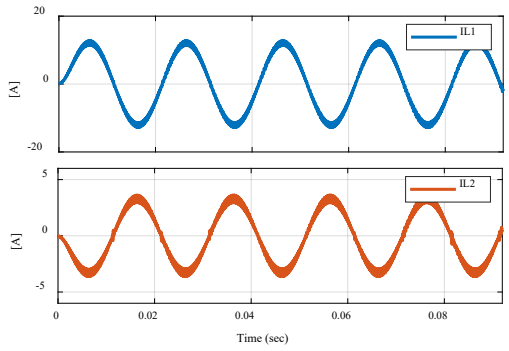


Figure 12: Current waveforms of the inductors L_1 and L_2

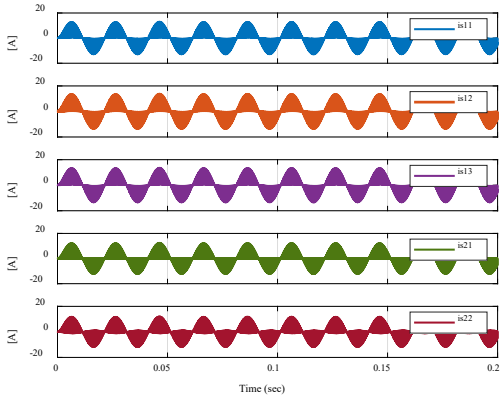


Figure 13: Current waveforms of the converter switches

8 Conclusion

In this paper, a modified topology for direct boost AC–AC converters was introduced and analyzed. The proposed converter, has simple configuration with only a single power stage and a boost cell, successfully enhanced the overall performance of the system. The main merits of the given topology include reducing losses caused by MOSFET body-diode reverse recovery, eliminating the need for dead time, and decreasing voltage and current stresses of power switches. These features not only simplify power control but also extend the lifetime of semiconductor devices. Finally, simulation results in MATLAB/Simulink demonstrated that the converter can operate with switching frequency of 50 kHz with high efficiency and stable performance. Furthermore, the results provide a foundation for future research on the development of advanced control algorithms and performance evaluation in practical systems.

Disclosure of Potential Conflicts of Interest

The Authors declare that there is no conflict of interest.

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